PATENT COOPERATION TREATY

E-MAILED 13 AUG 07

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:
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PCT

WRITTEN OPINION

(PCT Rule 66)

Date of Mailing (*day/month/year*)	17 AUG 2007
Applicant's or agent's file reference 040462WO	REPLY DUE within 2 months/days from the above date of mailing

International application No.	International filing date (*day/month/year*)	Priority date (*day/month/year*)
PCT/US03/06330	27 February 2003 (27.02.2003)	28 February 2002

International Patent Classification (IPC) or both national classification and IPC

IPC: H04Q 7/24(2006.01)
USPC: 370/338,349

Applicant

QUALCOMM INCORPORATED

1. This written opinion is the first (first, etc.) drawn by this International Preliminary Examining Authority.

2. This opinion contains indications relating to the following items:

- [x] I Basis of the opinion
- [ ] II Priority
- [ ] III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] IV Lack of unity of invention
- [x] V Reasoned statement under Rule 66.2 (a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] VI Certain documents cited
- [ ] VII Certain defects in the international application
- [ ] VIII Certain observations on the international application

3. The applicant is hereby invited to reply to this opinion.

When? See the time limit indicated above. ~~The applicant may, before the expiration of that time limit, request this Authority to grant an extension. See rule 66.2(d).~~

How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 66.8 and 66.9.

Also For an additional opportunity to submit amendments, see Rule 66.4.
For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4 *bis*.
For an informal communication with the examiner, see Rule 66.6

If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.

4. The final date by which the international preliminary examination report must be established according to Rule 69.2 is: 27 June 2005 (27.06.2005)

Name and mailing address of the IPEA/US Mail Stop PCT, Attn: IPEA/ US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	Authorized officer Toan Nguyen Telephone No. 571-272-2600

Form PCT/IPEA/408 (cover sheet)(July 1998)

WRITTEN OPINION

International application No.
PCT/US03/06330

I. Basis of the opinion

1. With regard to the elements of the international application:*

☒ the international application as originally filed

☒ the description:
pages 1-26, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of

☒ the claims:
pages 27-35, as originally filed
pages NONE, as amended (together with any statement) under Article 19
pages NONE, filed with the demand
pages NONE, filed with the letter of

☒ the drawings:
pages 1-16, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of

☐ the sequence listing part of the description:
pages NONE, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination(under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the written opinion was drawn on the basis of the sequence listing:

☐ contained in the international application in printed form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☒ The amendments have resulted in the cancellation of:

☒ the description, pages NONE

☒ the claims, Nos. NONE

☒ the drawings, sheets/fig NONE

5. ☐ This opinion has been drawn as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

* *Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this opinion as "originally filed."*

WRITTEN OPINION

International application No.
PCT/US03/06330

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims	1-45	YES
	Claims	46-52	NO
Inventive Step (IS)	Claims	NONE	YES
	Claims	1-52	NO
Industrial Applicability (IA)	Claims	1-52	YES
	Claims	NONE	NO

2. CITATIONS AND EXPLANATIONS
Please See Continuation Sheet

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TIME LIMIT:
The time limit set for response to a Written Opinion may not be extended. 37 CFR 1.484(d). Any response received after the expiration of the time limit set in the Written Opinion will not be considered in preparing the International Preliminary Examination Report.

V. 2. Citations and Explanations:
1. Claims 46 and 47 lack novelty under PCT Article 33(2) as being anticipated by Shacher et al. (US 5,671,223).
For claim 46, Shacher et al. disclose multichannel HDLC framing/deframing machine, comprising:
a deframer (figure 4, reference 112 Receiver Rx)) operative to receive a first block of data to be deframed, detect (figure 9, reference 308) for data bytes of a first set of specific values (col. 11 line 65 to col. 12 line 1), deframe the first data block in accordance with a particular deframing scheme, and provide deframed data for the first data block (figure 7, reference step 512, col. 10 line 27 and col. 12 lines 27-57);
a framer (figure 8, reference 534 Transmitter (Tx)) operative to receive a second block of data to be framed, detect (figure 14, reference 416) for data bytes of a second . set of specific values (col. 17 lines 22-23), frame (figure 8, reference step 534) the second data block in accordance with a particular framing scheme, and provide framed data for the second data block (col. 10 lines 50-51, and col. 16 lines 9); and
a controller (figure 3, reference 100) operative to direct deframing and framing by the deframer and framer, respectively (col. 6 lines 34-36).
For claim 47, Shacher et al. disclose further comprising:
a first buffer operative to store the deframed data from the deframer (figure 7, reference step 518, col. 10 line 35), and
a second buffer operative to store the framed data from the framer (figure 8, reference step 538, col. 10 lines 53-56).
2. Claims 48-52 lack novelty under PCT Article 33(2) as being anticipated by Zook (US 5,724,368).
For claims 48-52, Zook discloses cyclical redundancy check method and apparatus, comprising:
a latch operative to store an N-bit value (col. 1 line 61 to col. 3 line 16); and
plurality of (M) 1-bit CRC generators coupled in series and in a loop with the latch, wherein each 1-bit CRC generator is operative to receive an N-bit value from a preceding 1-bit CRC generator or the latch and a respective input data bit, scale N-1 least significant bits (LSBs) of the received N-bit value vy two, selectively add the scaled value with a predetermined value corresponding to a polynomial being implemented, and provide the selectively added results as an N-bit output for the 1-bit CRC generator (col. 4 line 11 to col. 13 line

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55).
3. Claims 1, 3, 8-14, 16, 21, 23-35, 39, and 42-45 lack an inventive step under PCT Article 33(3) as being obvious over Shacher et al. (US 5,671,223) in view of Hwang (US 6,788,652).
For claims 1 and 13, Shacher et al. disclose multichannel HDLC framing/deframing machine, comprising:
an input interface unit (figure 4, reference 120) operative to receive data to be deframed (col. 7 lines 10-11);
a detection unit (figure 9, reference 308) operative to evaluate each data byte from the input interface unit to detect for bytes of specific values (col. 11 line 65 to col. 12 line 1);
a state control unit (figure 9, reference 312) operative to provide a first set of control signals indicative of specific tasks to be performed for deframing based in part on the detected bytes of specific values (col. 12 lines 27-57).
However, Shacher et al. do not expressly disclose a conversion unit operative to deframe the received data based on the first set of control signals to provide deframed data. To include conversion unit operative to deframe the received data based on the first set of control signals to provide deframed data would have been obvious to one of ordinary skill in the art because Shacher et al. clearly teach at col. 12 lines 40-49 (see FIG. 10); "The Rx Main Transfer Control circuit 312 determines whether or not the bits shifted out of the PRE register 310 are shifted into the DATA register 330... Determination whether the machine is Inframe is according to the state diagram in FIG.10. Zero deletion is triggered when Inframe and five ones are detected (FONES) by the PST detection circuit 322."
Furthermore, Shacher et al. do not expressly disclose one or more Radio Link Protocol (RLP) packets. In an analogous art, Hwang discloses one or more Radio Link Protocol (RLP) packets (col. 6 lines 47-49).
Hwang discloses wherein the data block corresponds to a single Radio Link Protocol (RLP) packet (col. 6 lines 47-49 as set forth in claim 13).
To combine Hwang into Shacher et al. would not involve in an inventive step.
For claim 3, Shacher et al. disclose wherein the input interface unit (figure 4, reference 120) is operative to receive the data to be deframed in word of multiple bytes (col. 10 line 26) and, for each received word, provide one data byte at a time (col. 6 lines 45-46) for evaluation by the detection unit (col. 11 line 65 to col. 12 line 1).
For claim 8, Shacher et al. disclose wherein the conversion unit is operative to check each deframed packet based on a frame check sequence (FCS) value associated with the packet (col. 21, Table T-20, Field Name CR).
For claim 9, Shacher et al. disclose further comprising an output interface unit operative to provide a second set of control signals for storing the deframed data to an output buffer (col. 10 lines 33-35).
For claim 10, Shacher et al. disclose wherein the output interface unit is further operative to perform byte alignment of the deframed data provided by the deframer (col. 21, Table T-20, Field name NO).
For claim 11, Shacher et al. disclose wherein the deframer is operatYve to provide the deframed data in words of multiple bytes (Abstract line 10).
For claim 12, Shacher et al. disclose wherein the deframer is operative to deframe a block of data for each deframing operation (col. 4 lines 20-28).
For claim 14, Shacher et al. disclose a first register operative to store a value indicative of the number of deframed packets for the data block (col. 12 lines 60-64).
For claim 16, Shacher et al. disclose wherein the deframer is in one of a plurality of operating states at any given moment, and wherein the operating states include an idle state indicative of no deframing being performed and a process state indicative of deframing being performed (figure 10, col. 13 lines 30-34).
For claim 21, Shacher et al. disclose multichannel HDLC framing/deframing machine, comprising:
an input interface unit (figure 4, reference 120) operative to receive data to be framed (col. 7 lines 10-11);
a detection unit (figure 14, reference 416) operative to evaluate each data byte from the input interface unit to detect for bytes of specific values (col. 17 lines 22-23);
a state control unit (figure 14, reference 406) operative to provide a first set of control signals indicative of specific tasks to be performed for framing based in part on the detected bytes of specific values (col. 16 line 9).
However, Shacher et al. do not expressly disclose a conversion unit operative to frame the received data based on the first set of control signals and in accordance with a particular framing scheme to provide framed data. To include the conversion unit operative to frame the received data based on the first set of control signals and in accordance with a particular framing scheme to provide framed data would have been obvious to one of ordinary skill in the art because Shacher et al. clearly teach at col. 16 lines 7-9 (see FIG.14), "This signal is one of the input signals to the Select Circuit 406, directing the Select Circuit 406 to supply a zero for zero insertion as the next bit shifted into DTA 420 and DATAO 422, unless in transparent mode."
Furthermore, Shacher et al. do not expressly disclose one or more Radio Link Protocol (RLP) packets. In an analogous art, Hwang discloses one or more Radio Link Protocol (RLP) packets (col. 6 lines 47-49).

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To combine Hwang into Shacher et al. would not involve in an inventive step.
For claim 23, Shacher et al. disclose wherein the input interface unit (figure 4, reference 120) is operative to receive the data to be framed in word of multiple bytes (col. 10 line 53) and, for each received word, provide one data byte at a time (figure 14, reference 416) for evaluation by the detection unit (col. 17 lines 22-23).
For claims 24-26, Shacher et al. disclose wherein the conversion unit is further operative to insert a flag byte in response to receiving a first command (col. 16 lines 6-9).
For claim 27, Shacher et al. disclose further comprising an output interface unit operative to provide a second set of control signals for storing the framed data to an output buffer (col. 10 lines 53-55).
For claim 28, Shacher et al. disclose wherein the output interface unit is further operative to perform byte alignment of the framed data provided by the framer (col. 21, Table T-20, Field name NO).
For claim 29, Shacher et al. disclose wherein the output interface unit is operative to provide the framed data in words of multiple bytes (col. 10 lines 53-55).
For claims 30-31, Shacher et al. disclose wherein the framer is operative to frame a block of data for each framing operation (col. 4 lines 20-28).
For claims 32-34, Shacher et al. disclose wherein the framer is in one of a plurality of operating states at any given moment, and wherein the operating states include an idle state indicative of no framing being performed and a process state indicative of framing being performed (col. 17 lines 10-30).
For claim 35, Shacher et al. disclose a first register operative to store a value indicative of the number of framed packets for the data block (col. 16 lines 60-62).
For claim 39, Shacher et al. disclose multichannel HDLC framing/deframing machine, comprising:
a deframer (figure 4, reference 112 Receiver Rx)) operative to receive a first block of data to be deframed, detect (figure 9, reference 308) for data bytes of a first set of specific values (col. 11 line 65 to col. 12 line 1), deframe the first data block in accordance with a particular deframing schemes and provide deframed data for the first data block (figure 7, reference step 512, col. 10 line 27 and col. 12 lines 27-57); and
a framer (figure 8, reference 534 Transmitter (Tx)) operative to receive a second block of data to be framed, detect (figure 14, reference 416) for data bytes of a second set of specific values (col. 17 lines 22-23), frame (figure 8, reference step 534) the second data block in accordance with a particular framing scheme, and provide framed data for the second data block (col. 10 lines 50-51, and col. 16 lines 9).
However, Shacher et al. do not expressly disclose a Radio Link Protocol (RLP) packet. In an analogous art, Hwang discloses a Radio Link Protocol (RLP) packet (col. 6 lines 47-49).
To combine Hwang into Shacher et al. would not involve in an inventive step.
For claim 42, Shacher et al. disclose further comprising:
a first buffer operative to store the deframed data from the deframer (figure 7, reference step 518, col. 10 line 35).
For claim 43, Shacher et al. disclose further comprising:
a second buffer operative to store the framed data from the framer (figure 8, reference step 538, col. 10 lines 53-55).
For claim 44, Shacher et al. disclose further comprising: at least one buffer interface unit (figre 22, reference 98) operable to retrieve the deframed data stored in the first buffer or the framed data stored in the second buffer (col. 24 lines 64-65).
For claim 45, Shacher et al. disclose wherein the deframer and framer are each operated in one of a plurality of possible operating states (figures 7 and 8, col. 10 lines 26-30 and col. 10 lines 50-52).
4. Claims 2, 15, 17, 22, and 40-41 lack an inventive step under PCT Article 33(3) as being obvious over Shacher et al. (US 5,671,223) in view of Hwang (Us 6,788,652) further in view of W. Simpson, RFC 1662.
For claim 2, 15, 17,22, 40, and 41, Shacher et al. in view of Hwang do not expressly disclose wherein the data to be deframed conforms to a frame format defined by RFC1662. In an analogous art, W. Simpson discloses wherein the data to be deframed conforms to a frame format defined by RFC1662 (See 3.1.Frame Format, page 5).
W. Simpson discloses operative to provide a first header for a start of the block (see 3.1 Frame Format as set forth in claim 15), wherein the operating states include an escape state indicative of processing for an escape byte and a header state indicative of generation of a header for the deframed data (section 3.1 Frame Format as set forth in claim 17); further wherein the framed data conforms to a frame format defined by RFC1662 (See 3.1. Frame Format, page 5 as set forth in claim 22), wherein the data to be deframed in the first data block and the framed data for the second data block each have a format defined by RFC1662 (See 3.1. Frame Format, page 5 as set forth in claim 40), at least one frame check sequence (FCS) generator operative to generate an FCS value for each packet to be framed or deframed (See C.1.FSC table generator, page 18 as set forth in

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claim 41).
To combine W. Simpson into Shacher et al. would not involve in an inventive step.
5. Claims 4-7 lack an inventive step under PCT Article 33(3) as being obvious over Shacher et al. (US 5,671,223) in view of Hwang (Us 6,788,652) further in view of Aggarwal et al. (US 6,249,525).
For claims 4-7, Shacher et al. disclose wherein the detection unit is operative to detect for flag byte in the received data (col. 11 line 67 to col. 12 line 1).
However, Shacher et al. in view of Hwang do not expressly disclose to detect for escape byte in the received data. In an analogous art, Aggarwal et al. disclose to detect for escape byte in the received data (col. 1 line 43), wherein the conversion unit is further operative to remove flag and escape bytes in the received data (col. 13 line 66 to col. 14 line 14 as set forth in claim 5); wherein the conversion unit is further operative to un-escape a data byte following each detected escape byte in the received data (col. 13 line 66 to col. 14 line 14 as set forth in claim 6), operative to provide a word for each detected flag byte in the received data (col. 1 lines 43-44, and col. 13 line 66 to col. 14 line 14 as set forth in claim 7).
To combine Aggarwal et al. into Shacher et al. would not involve in an inventive step.
6. Claims 18-20, 36 and 38 lack an inventive step under PCT Article 33(3) as being obvious over Shacher et al. (US 5,671,223) in view of Aggarwal et al. (US 6,249,525) further in view of W. Simpson, RFC 1662.
For claim 18, Shacher et al. disclose multichannel HDLC framing/deframing machine, comprising:
an input interface unit (figure 4, reference 120) operative to receive an RLP packet of data to be framed, one word at a time, and for each received word provide one data byte at a time for subsequent processing (col. 7 lines 10-11);
a detection unit (figure 9, reference 308) operative to evaluate each data byte from the input interface unit (col. 11 line 65 to col. 12 line 1).
Shacher et al. do not expressly disclose a conversion unit operative to process each data byte from the interface unit. To include a conversion unit operative to process each data byte from the interface unit would have been obvious to one of ordinary skill in the art because Shacher et al. clearly teach at col. 12 lines 40-49 (see FIG. 10), "The Rx Main Transfer Control Unit circuit 312 determines whether or not the bits shifted out of the register 310 are shifted into the DATA register 330...Determination whether the machine is inframe is according to the state diagram in FIG. 10. Zero deletion is triggered when inframe and five ones are detected (FONES) by the PST detection circuit 322." However, Shacher et al. do not expressly disclose removing flag and escape bytes, un-escaping a data byte following each escape byte, providing a header word for each flag byte, and checking each deframed packet based on a frame check sequence (FCS) value associated with the packet; and an output interface unit operative to provide deframe data; and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC 1662. In an analogous art, Aggarwal et al. disclose removing flag and escape bytes, un-escaping a data byte following each escape byte, providing a word for each flag byte (col. 1 lines 43-44, and col. 13 line 66 to col. 14 line 14).
To combine Aggarwal et al. into Shacher et al. would not involve in an inventive step.
Furthermore, Shacher et al. in view of Aggarwal et al do not expressly disclose providing a header word for each flag byte, and checking each deframed packet based on a frame check sequence (FCS) value associated with packet; and an output interface unit operative to provide deframed data; and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC 1662. In an analogous art, W. Simpson disclose providing a header word for each flag byte (page 4, section 3.1 Frame Format), and checking each deframed packet based on a frame check sequence (FCS) value associated with packet (page 5, section 3.1 Frame Format); and an output interface unit operative to provide deframed data; and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC 1662 (see W. Simpson, RFC: 1662).
To combine W. Simpson into Shacher et al. would not involve in an inventive step.
For claim 19, Shacher et al. disclose multichannel HDLC framing/deframing machine, comprising:
an input interface unit (figure 4, reference 120) operative to receive an RLP packet of data to be framed, one word at a time, and for each received word provide one data byte at a time for subsequent processing (col. 7 lines 10-11);
a detection unit (figure 9, reference 308) operative to evaluate each data byte from the input interface unit (col. 11 line 65 to col. 12 line 1).
Shacher et al. do not expressly disclose a conversion unit operative to process each data byte from the interface unit. To include a conversion unit operative to process each data byte from the interface unit would have been obvious to one of ordinary skill in the art because Shacher et al. clearly teach at col. 12 lines 40-49 (see FIG. 10), "The Rx Main Transfer Control Unit circuit 312 determines whether or not the bits shifted out of the register 310 are shifted into the DATA register 330...Determination whether the machine is inframe is

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according to the state diagram in FIG. 10. Zero deletion is triggered when Inframe and five ones are detected (FONES) by the PST detection circuit 322." However, Shacher et al. do not expressly disclose removing flag and escape bytes, un-escaping a data byte following each escape byte, providing a header word for each flag byte, and checking each deframed packet based on a frame check sequence (FCS) value associated with the packet; and an output interface unit operative to provide deframe data; and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC 1662. In an analogous art, Aggarwal et al. disclose removing flag and escape bytes, un-escaping a data byte following each escape byte, providing a word for each flag byte (col. 1 lines 43-44, and col. 13 line 66 to col. 14 line 14).
To combine Aggarwal et al. into Shacher et al. would not involve in an inventive step.
Furthermore, Shacher et al. in view of Aggarwal et al do not expressly disclose providing a header word for each flag byte, and checking each deframed packet based on a frame check sequence (FCS) value associated with packet; and an output interface unit operative to provide deframed data; and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC 1662. In an analogous art, W. Simpson disclose providing a header word for each flag byte (page 4, section 3.1 Frame Format), and checking each deframed packet based on a frame check sequence (FCS) value associated with packet (page 5, section 3.1 Frame Format); and an output interface unit operative to provide deframed data; and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC 1662 (see W. Simpson, RFC: 1662).
To combine W. Simpson into Shacher et al. would not involve in an inventive step.
For claim 20, Shacher et al. disclose multichannel HDLC framing/deframing machine, comprising:
receiving the RLP packet, one word at a time; evaluating each byte of each received word (col. 7 lines 10-11);
providing status signals indicative of each detected flag byte (col. 11 line 65 to col. 12 line 1).
However, Shacher et al. do not expressly disclose removing the flag and escape bytes; un-escaping a data byte following each detected escape byte; checking each PPP packet based on an FCS value associated with the packet; and providing deframed data. In an analogous art, Aggarwal et al. disclose removing the flag and escape bytes; un-escaping a data byte following each detected escape byte (col. 1 lines 43-44, and col. 13 line 66 to col. 14 line 14).
To combine Aggarwal et al. into Shacher et al. would not involve in an inventive step.
Furthermore, Shacher et al. in view of Aggarwal et al. do not expressly disclose checking each PPP packet based on an FCS value associated with the packet; and providing deframed data. In an analogous art, W. Simpson discloses checking each PPP packet based on an FCS value associated with the packet; and providing deframed data (page 5, section 3.1 Frame Format).
To combine W. Simpson into Shacher et al. would not involve in an inventive step.
For claim 36, Shacher et al. disclose multichannel HDLC framing/deframing machine, comprising:
an input interface unit (figure 4, reference 120) operative to receive an RLP packet of data to be framed, one word at a time, and for each received word provide one data byte at a time for subsequent processing (col. 7 lines 10-11);
a detection unit (figure 9, reference 308) operative to evaluate each data byte from the input interface unit (col. 11 line 65 to col. 12 line 1).
Shacher et al. do not expressly disclose a conversion unit operative to process each data byte from the interface unit. To include a conversion unit operative to process each data byte from the interface unit would have been obvious to one of ordinary skill in the art because Shacher et al. clearly teach at col. 12 lines 40-49 (see FIG. 10), "The Rx Main Transfer Control Unit circuit 312 determines whether or not the bits shifted out of the register 310 are shifted into the DATA register 330...Determination whether the machine is Inframe is according to the state diagram in FIG. 10. Zero deletion is triggered when Inframe and five ones are detected (FONES) by the PST detection circuit 322." However, Shacher et al. do not expressly disclose removing flag and escape bytes, un-escaping a data byte following each escape byte, providing a header word for each flag byte, and checking each deframed packet based on a frame check sequence (FCS) value associated with the packet; and an output interface unit operative to provide deframe data; and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC 1662. In an analogous art, Aggarwal et al. disclose removing flag and escape bytes, un-escaping a data byte following each escape byte, providing a word for each flag byte (col. 1 lines 43-44, and col. 13 line 66 to col. 14 line 14).
To combine Aggarwal et al. into Shacher et al. would not involve in an inventive step.
Furthermore, Shacher et al. in view of Aggarwal et al do not expressly disclose providing a header word for each flag byte, and checking each deframed packet based on a frame check sequence (FCS) value associated with packet; and an output interface unit operative to provide deframed data; and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC 1662. In an analogous art, W. Simpson disclose providing a header word for

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each flag byte (page 4, section 3.1 Frame Format), and checking each deframed packet based on a frame check sequence (FCS) value associated with packet (page 5, section 3.1 Frame Format); and an output interface unit operative to provide deframed data; and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC 1662 (see W. Simpson, RFC: 1662).

To combine W. Simpson into Shacher et al. would not involve in an inventive step.

For claim 37, Shacher et al. disclose multichannel HDLC framing/deframing machine, comprising:

an input interface unit (figure 4, reference 120) operative to receive an RLP packet of data to be framed, one word at a time, and for each received word provide one data byte at a time for subsequent processing (col. 7 lines 10-11);

a detection unit (figure 9, reference 308) operative to evaluate each data byte from the input interface unit (col. 11 line 65 to col. 12 line 1).

Shacher et al. do not expressly disclose a conversion unit operative to process each data byte from the interface unit. To include a conversion unit operative to process each data byte from the interface unit would have been obvious to one of ordinary skill in the art because Shacher et al. clearly teach at col. 12 lines 40-49 (see FIG. 10), "The Rx Main Transfer Control Unit circuit 312 determines whether or not the bits shifted out of the register 310 are shifted into the DATA register 330...Determination whether the machine is Inframe is according to the state diagram in FIG. 10. Zero deletion is triggered when Inframe and five ones are detected (FONES) by the PST detection circuit 322." However, Shacher et al. do not expressly disclose removing flag and escape bytes, un-escaping a data byte following each escape byte, providing a header word for each flag byte, and checking each deframed packet based on a frame check sequence (FCS) value associated with the packet; and an output interface unit operative to provide deframe data; and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC 1662. In an analogous art, Aggarwal et al. disclose removing flag and escape bytes, un-escaping a data byte following each escape byte, providing a word for each flag byte (col. 1 lines 43-44, and col. 13 line 66 to col. 14 line 14).

To combine Aggarwal et al. into Shacher et al. would not involve in an inventive step.

Furthermore, Shacher et al. in view of Aggarwal et al do not expressly disclose providing a header word for each flag byte, and checking each deframed packet based on a frame check sequence (FCS) value associated with packet; and an output interface unit operative to provide deframed data; and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC 1662. In an analogous art, W. Simpson disclose providing a header word for each flag byte (page 4, section 3.1 Frame Format), and checking each deframed packet based on a frame check sequence (FCS) value associated with packet (page 5, section 3.1 Frame Format); and an output interface unit operative to provide deframed data; and wherein the RLP packet includes one or more complete or partial PPP packets having a format defined by RFC 1662 (see W. Simpson, RFC: 1662).

To combine W. Simpson into Shacher et al. would not involve in an inventive step.

For claim 38, Shacher et al. disclose multichannel HDLC framing/deframing machine, comprising:

receiving the packet, one word at a time; evaluating each byte of each received word to detect for bytes (col. 7 lines 10-11);

providing status signals indicative of each data byte (col. 11 line 65 to col. 12 line 1). However, Shacher et al. do not expressly disclose inserting escape bytes for each data byte to be escaped and escaping the data byte; inserting a flag byte in response to receiving a flag insert command; inserting an FCS value in response to receiving an FCS insert command; and providing framed data having the format defined by RFC 1662. In an analogous art, Aggarwal et al. disclose inserting escape bytes for each data byte to be escaped and escaping the data byte; inserting a flag byte in response to receiving a flag insert command (col. 13 line 66 to col. 14 line 14).

To combine Aggarwal et al. into Shacher et al. would not involve in an inventive step.

Furthermore, Shacher et al. in view of Aggarwal et al. do not expressly disclose inserting an FCS value in response to receiving an FCS insert command; and providing framed data having the format defined by RFC 1662. In an analogous art, W. Simpson discloses inserting an FCS value in response to receiving an FCS insert command; and providing framed data having the format defined by RFC 1662 (section 3.1 Frame Format).

To combine W. Simpson into Shacher et al. would not involve in an inventive step.

---------- NEW CITATIONS ----------

US 5,671,223 A (SHACHAR et al) 23 September 1997, see the entire document.

US 6,249,525 A (AGGARWAL et al) 19 June 2001, see the entire document.

W. Simpson, PPP in HDLC-like Framing, Network Working Group Request for Comments: 1662, July 1994, pages 1-24.